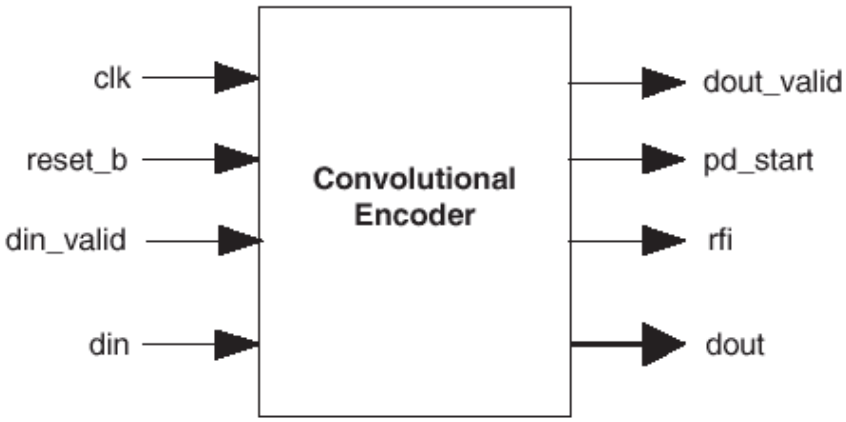
Convolutional Encoder

Overview

Convolutional encoding is a process of adding redundancy to a signal stream. Lattice's Convolutional Encoder core is a parameterizable core for convolutional encoding of a continuous input data stream. The core allows variable code rates, constraint lengths and generator polynomials. The core also supports puncturing. Puncturing enables a large range of transmission rates and reduces the bandwidth requirement on the channel.



Features

- Parameterizable continuous convolutional encoder
- Available for ORCA Series 4 FPGA and FPSC devices.
- Parameterizable constraint length from 3 to 12
- Parameterizable convolutional codes
- Parameterizable puncture codes
- Puncturing input rates from 2 to 12
- Puncturing output rates from 2 to 23

Evaluation Configurations

Convolutional Encoder Evaluation Configurations avaiable for ORCA4 FPGAs and FPSCs[1]

Config #	ORCA4 PFUs[2]	LUTs	Registers	External I/Os	SysMem EBRs	f_{MAX} (MHz)	Latency[3]
conv_enco_o4_1_001.lpc	**4**	6	16	7	N/A	342	3

[1] Performance and utilization characteristics using ispLEVER software and targeting the OR4E02, package BA352, speed 2.

[2] Programmable Function Unit (PFU) is a standard logic block of Lattice FPGA devices. For more information, check the data sheet of the device.

[3] The latency values are for din to dout with din_valid is high whenever rfi is high. The din to dout latency relationship can be explained as follows. For non-punctured encoders, the latency value is 3 when constraint length is greater than 4, otherwise the value is 2. For punctured encoders, the latency value is (output rate + 6) when constraint length is greater than 4, otherwise the value is (output rate + 4).

Convolutional Encoder Evaluation Configurations avaiable for ispXPGA[1]

Configuration	XPGA PFUs[2]	LUT-4s	Registers	External I/Os	SysMem EBRs	f_{MAX} (MHz)	Latency[3]
conv_enco_xp_1_001.lpc	**6**	6	22	7	N/A	510	3

[1] Performance and utilization characteristics using ispLEVER software and targeting the LFX1200B, package FE680, speed 4.

[2] Programmable Function Unit (PFU) is a standard logic block of Lattice FPGA devices. For more information, check the data sheet of the device.

[3] The latency values are for din to dout with din_valid is high whenever rfi is high. The din to dout latency relationship can be explained as follows: For Non-punctured encoders, the latency value is 3 when Constraint Length is greater than 4 or else the value is 2. For punctured encoders, the latency value is (Output Rate + 6) when Constraint Length is greater than 4 or else the value is (Output Rate + 4).

Ordering Information

Part Numbers: For ORCA4: CONV-ENCO-O4-N1
For XPGA: CONV-ENCO-XP-N1

To find out how to purchase the Convolutional Encoder IP Core, please contact your **local Lattice Sales Office**.