High Performance Regulators for PCs

Nch FET Ultra LDO for PC Chipsets

BD3507HFV

No.10030EAT31

●Description

The BD3507HFV is suited for power supply for chipset bus. Though small in size, BD3507HFV adopts power PKG with radiation fins, and it therefore can be used for a regulator up to 550mA. Because it adopts Nch MOSFET and can form a ultra LDO power supply of R_{ON}=300mΩ (TYP), BD3507HFV can compose a high-efficiency system, though it is of a linear type power supply. The output voltage can be set by VREF terminal and can be synchronized with other power supply.
In addition, it can be used as a high side switch (R_{ON} = 300mΩ/Io = 550mA) of low-voltage power supply line.
Because ceramic capacitors can be used for output capacitors, BD3507HFV contributes to downsizing and reduced thickness not only of IC but also of sets.

●Features

1) Built-in high-accuracy buffer circuit (can be set to 0.65-2.7V)
2) Adoption of ceramic capacitors
3) Built-in enable function (0μA at standby)
4) Built-in current limiting circuit (550mA Max)
5) Built-in under voltage lockout circuit (UVLO)
6) Built-in thermal shutdown circuit (TSD)
7) Adoption of ultra-small-size high-power HVSOF6 package (3.0 x 1.6 x 0.75 mm)

●Applications

Notebook PC, desktop PC, digital camera, digital home appliances

●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Input Voltage1	V_{CC}	6.0 *1 *2	V
Input Voltage2	V_{IN}	6.0 *1 *2	V
Enable Input Voltage	V_{EN}	6.0 *1 *2	V
Power Dissipation1	Pd1	512.5 *3	mW
Power Dissipation2	Pd2	850.0 *4	mW
Operating Temperature Range	Topr	-10～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 However, not exceeding Pd.
*2 Maximum rating that can stand instantaneous voltage application such as surge, back EMF, or continuous pulse application whose duty ratio lowers 10%.
*3 In the case of Ta≥25°C (when mounting to 70mmx70mmx1.6mm glass epoxy substrate), derated at 4.1 mW/°C.
*4 In the case of Ta≥25°C (when mounting to 70mmx70mmx1.6mm glass epoxy substrate (copper foil area: 100 mm^2)), derated at 6.8 mW/°C.

●Operating Conditions (Ta=25℃)

Parameter	Symbol	Ratings		Unit
		MIN	MAX	
Input Voltage1	V_{CC}	4.5	5.5	V
Input Voltage2	V_{IN}	1.2	Vcc-1	V
VREF Setup Voltage	V_{REF}	0.65	2.7	V
EN Input Voltage	V_{EN}	-0.3	5.5	V
Output Current	I_O	0	550	mA

★ No radiation-resistant design is adopted for the present product.

●**Electrical Characteristics (unless otherwise noted, Ta=25℃, V_{CC}=5V, V_{IN}=1.8V, V_{REF}=1.2V, V_{EN}=3V)**

Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
Bias Current	I_{CC}	-	0.4	0.7	mA	
Standby Current1	I_{STB}	-	0	10	μA	V_{EN}=0V
Standby Current2	I_{INSTB}	-	0	10	μA	V_{EN}=0V
Output Voltage1	Vo1	1.188	1.200	1.212	V	Io=0mA
Output Voltage2	Vo2	1.188	1.200	1.212	V	Io=300mA
Output Voltage3	Vo3	1.176	1.200	1.224	V	Io=0mA to 550mA Vcc=4.5V to 5.5V Ta=-10℃ to 100℃ *5
Output Voltage4	Vo4	2.475	2.500	2.525	V	V_{IN}=3.3V,V_{REF}=2.5V Io=0mA
Output Voltage5	Vo5	2.475	2.500	2.525	V	V_{IN}=3.3V,V_{REF}=2.5V Io=300mA
Output Voltage6	Vo6	2.450	2.500	2.550	V	V_{IN}=3.3V,V_{REF}=2.5V Io=0mA to 550mA Vcc=4.5V to 5.5V Ta=-10℃ to 100℃ *5
Over Current Protect	I_{CL}	600	-	-	mA	
Output ON Resistance	R_{ON}	-	300	550	mΩ	
High Level Enable Input Voltage	EN_{High}	2.0	-	-	V	EN:Sweep-up
Low Level Enable Input Voltage	ENLOW	-0.2	-	0.8	V	EN:Sweep-down
Enable Pin Input Current	I_{EN}	-	7	10	μA	V_{EN}=3V
UVLO OFF Voltage	V_{UVLO}	3.5	3.8	4.1	V	Vcc:Sweep-up
UVLO Hysteresis Voltage	V_{HYS}	100	160	220	mV	Vcc:Sweep-down
VREF Pin Bias Current	I_{VREF}	-0.1	-	0.1	μA	V_{REF}=0→2.7 V *5
VREF Discharge ON Resistance	R_{ONREF}	-	1.0	2.0	kΩ	
Output Discharge ON Resistance	R_{ONDIS}	-	0.1	0.3	kΩ	

*5 Design Guarantee

●Reference Data

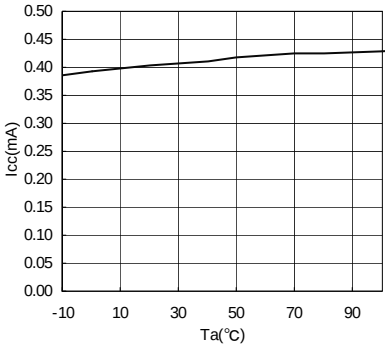


Fig.1 Ta-Icc (Vcc)

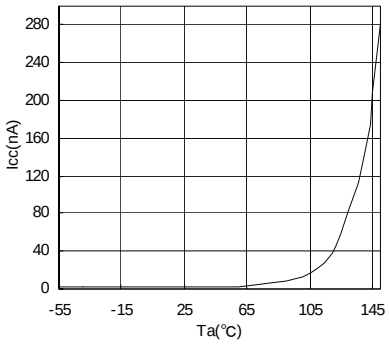


Fig.2 Ta-ISTB (Vcc)

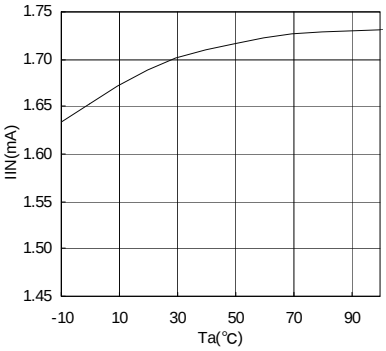


Fig.3 Ta-IIN (VIN)

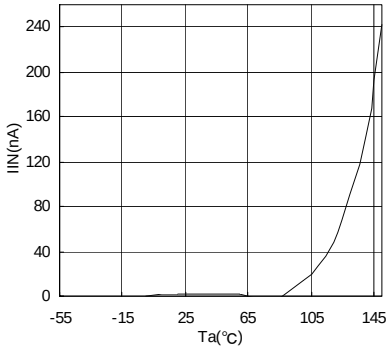


Fig.4 Ta-IINSTB (VIN)

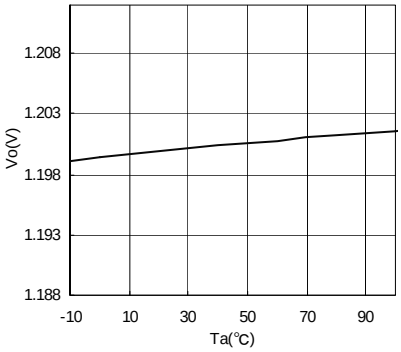


Fig.5 Ta-Vo

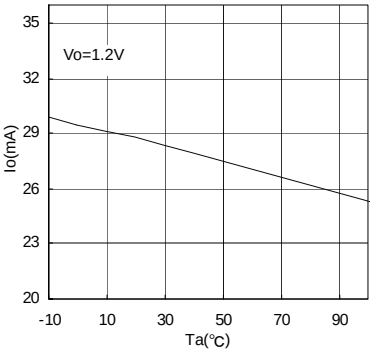


Fig.6 Ta-IODIS

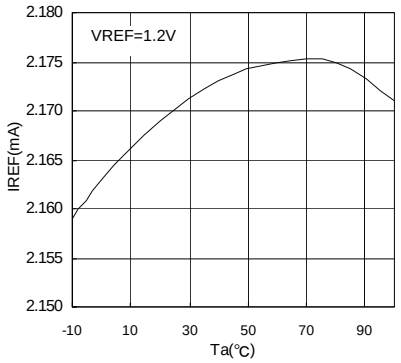


Fig.7 Ta-IrefDIS

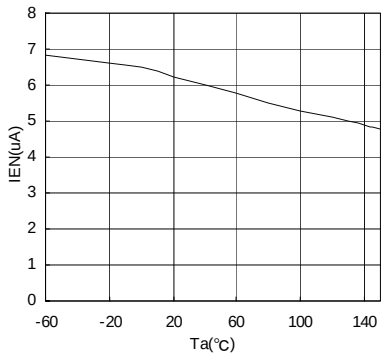


Fig.8 Ta-IEN

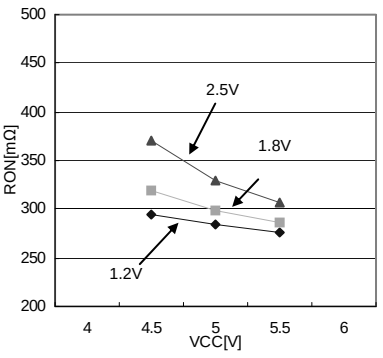


Fig.9 Vcc-Ron

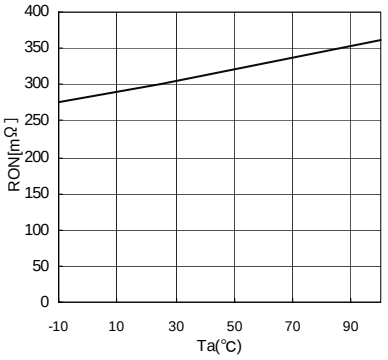


Fig.10 Ta-Ron

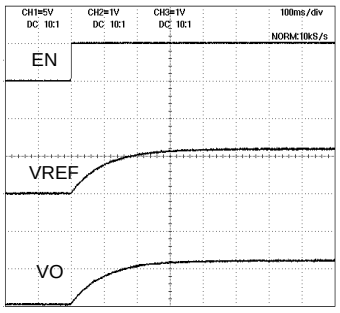


Fig.11 Startup Wave Form

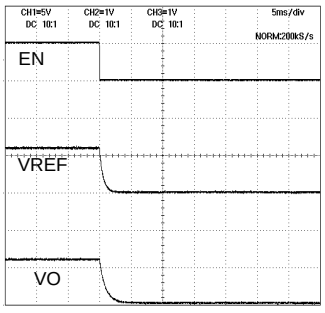


Fig.12 Shutdown Wave Form

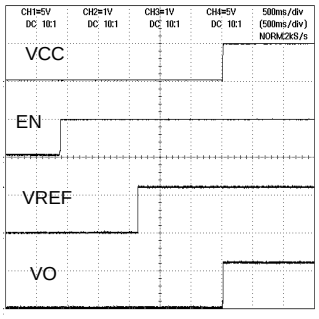


Fig.13 Input Sequence 1

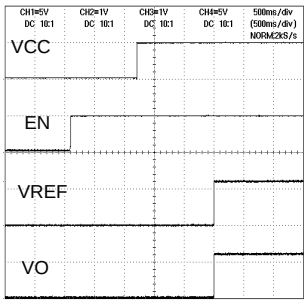


Fig.14 Input Sequence 2

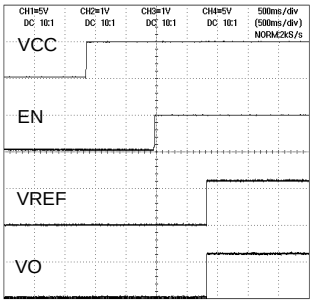


Fig.15 Input Sequence 3

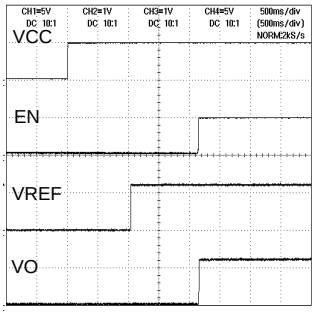


Fig.16 Input Sequence 4

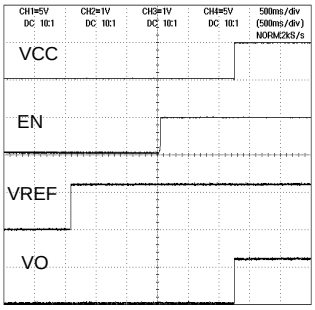


Fig.17 Input Sequence 5

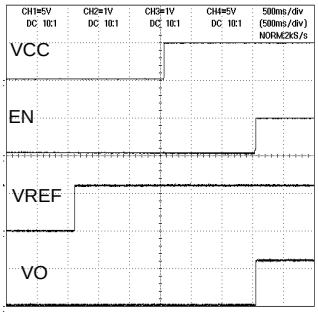


Fig.18 Input Sequence 6

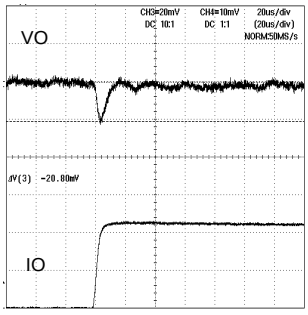


Fig.19 Transient Response
(0→550mA/μs)

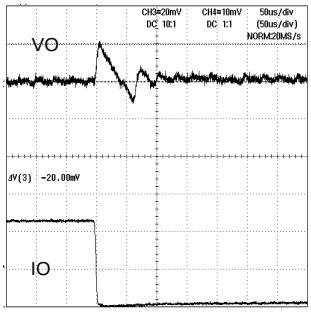
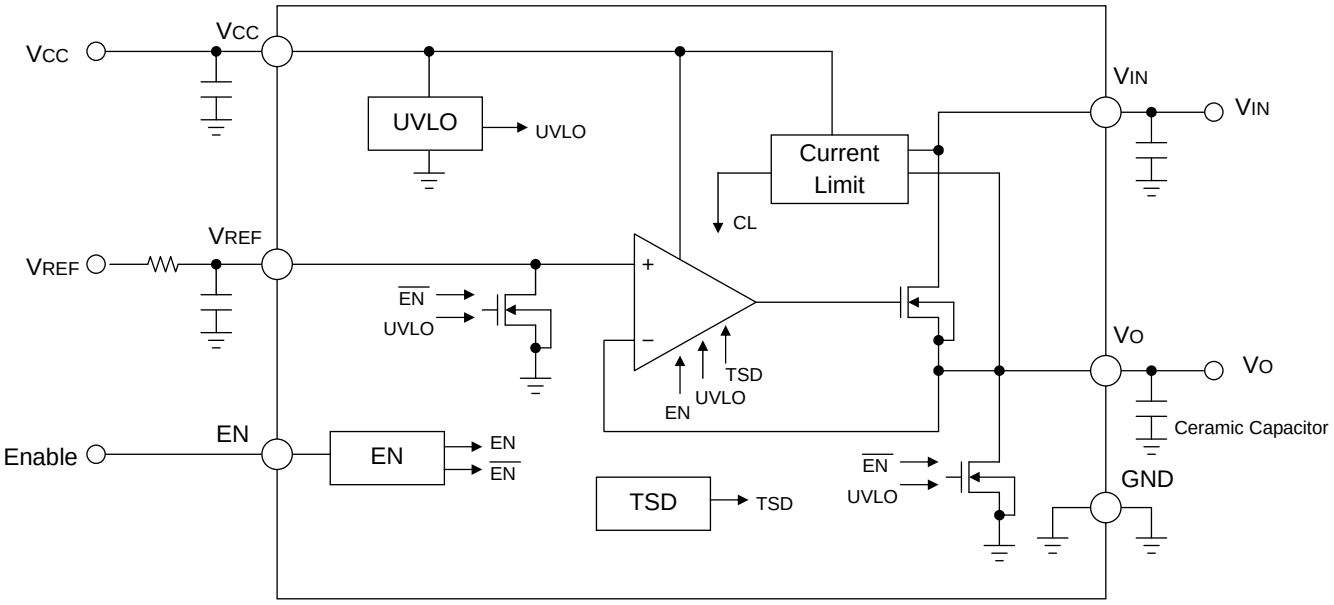


Fig.20 Transient Response
(550→0mA/μs)

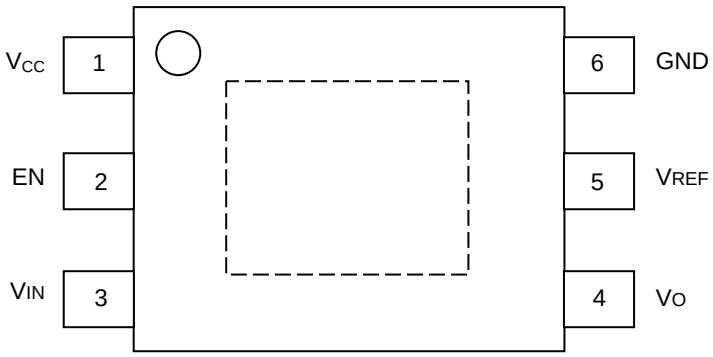
●Block Diagram



●Pin Function

Pin No.	Pin Name	PIN Function
1	V_{CC}	VCC Pin
2	EN	Enable Input Pin
3	V_{IN}	Input Voltage Pin
4	Vo	Output Pin
5	V_{REF}	Reference Voltage Input Pin
6	GND	Ground Pin

●Pin Configration



●Block Function

・AMP
An error amplifier that compares reference voltage (V_{REF}) to Vo and drives Nch FET (Ron=300 mΩ) of output. The frequency characteristics are optimized so that ceramic capacitors can be used for output capacitors and high-speed transient response can be achieved. The input voltage range at the AMP section is GND-2.7V and the output voltage range of the AMP section is GND-VCC. At the time of EN OFF or UVLO, the output is brought to the LOW level and the output NchFET is turned OFF.

・EN
By the logic input pin, regulator ON/OFF is controlled. At the time of OFF, the circuit current is controlled to be 0μA to reduce the standby current consumption of the apparatus. In addition, EN turns ON FET that can discharge V_{REF} and Vo and removes excess electric charge to prevent maloperation of IC on the load side. Since there is no electrical connection with the Vcc terminal as is the case of Di for electrostatic measures, it does not depend on the input sequence.

・UVLO
UVLO turned OFF output to prevent output voltage from making maloperation at the time of Vcc reduced voltage. Same as EN, UVLO discharges VREF and Vo. When voltage exceeds the threshold voltage (TYP 3.8V), UVLO starts output.

・CURRENT LIMIT
In the event the output current that exceeds the current (0.6A or more) set inside the IC flows when output is turned ON, output voltage is attenuated to protect the IC on the load side. When current reduces, output voltage returns to the set voltage.

・SOFT START
Adding external resistor and capacitor to V_{REF} pin can achieve soft-start. By the time constant that is determined by the time constant of CR, V_{REF} pin becomes dull, and output rises in synchronism with V_{REF} pin. Overshoot of output voltage or inrush current can be prevented.

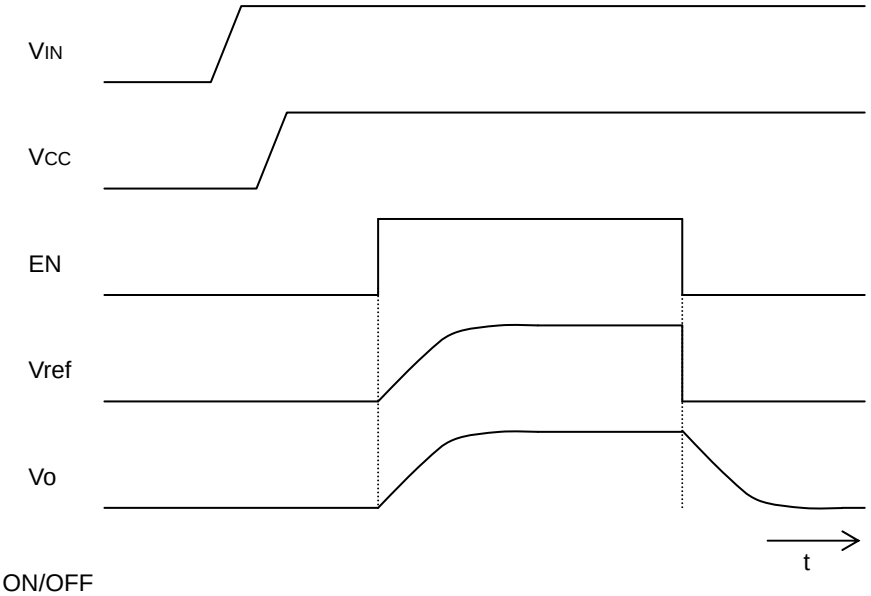
・VREF
VREF is a reference voltage input pin and sets output voltage. Since there is no electrical connection with the Vcc terminal as is the case of Di for electrostatic measures, it does not depend on the input sequence.

・TSD(Thermal Shut down)
In order to prevent thermal breakdown and thermal runaway of the IC, the output is turned OFF when chip temperature becomes high. In addition, when temperature returns to the specified temperature, the output is recovered. However, since the temperature protection circuit is originally built in to protect the IC itself, thermal design within Tj(max) is requested.

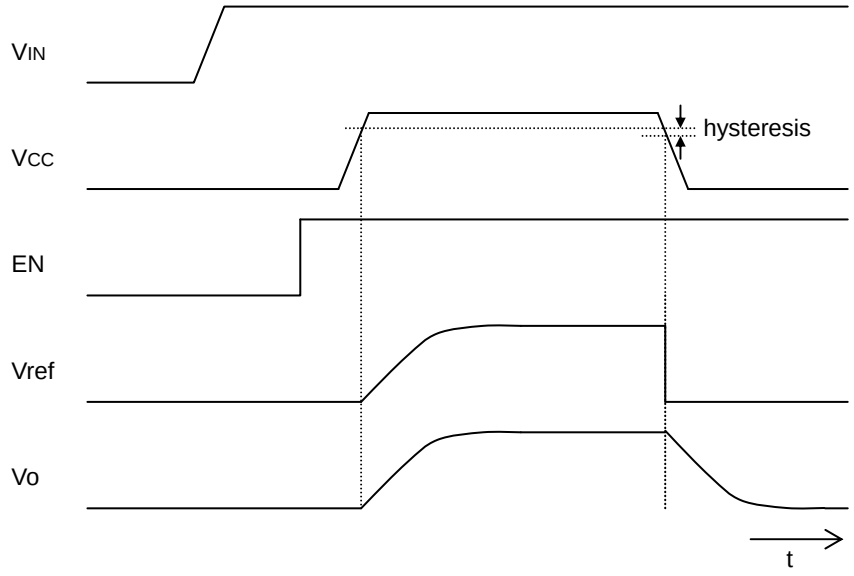
・VIN
This is a large-current supply line. The VIN terminal is connected to the rain of output NchFET. Since there is no electrical connection with the Vcc terminal as is the case of Di for electrostatic measures, it does not depend on the input sequence. However, because there is body Di of output Nch FET between VIN and Vo, there is electrical connection (Di-connection) between VIN and Vo. Consequently, when the output is turned ON/OFF by VIN, reverse current flows from Vo to VIN, to which care must be taken.

●**Timing Chart**

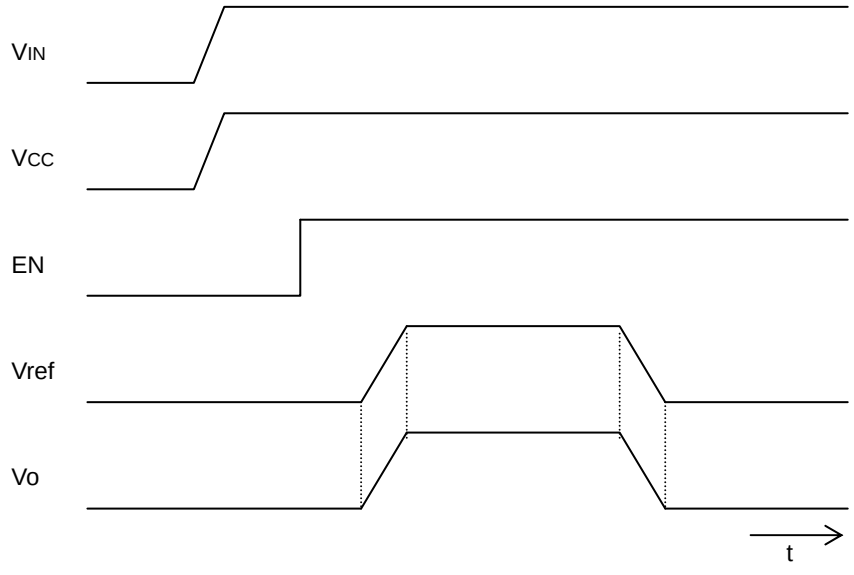
EN ON/OFF



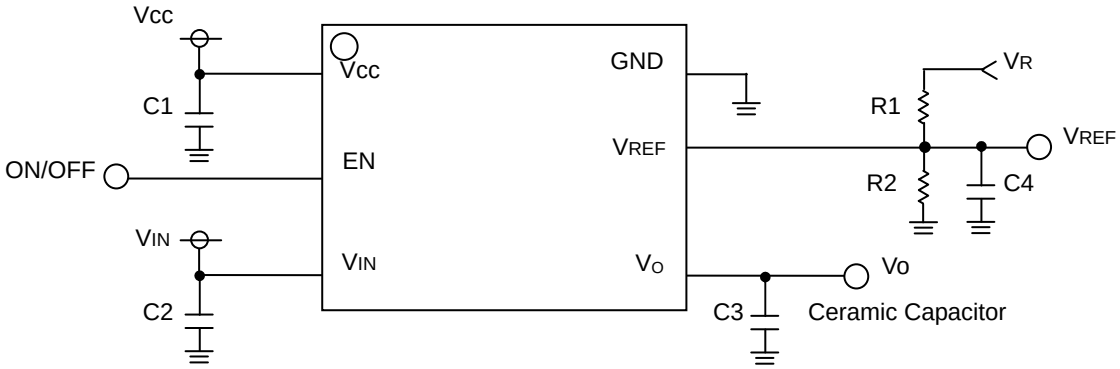
V_{CC} ON/OFF



Vref Synchronous Action



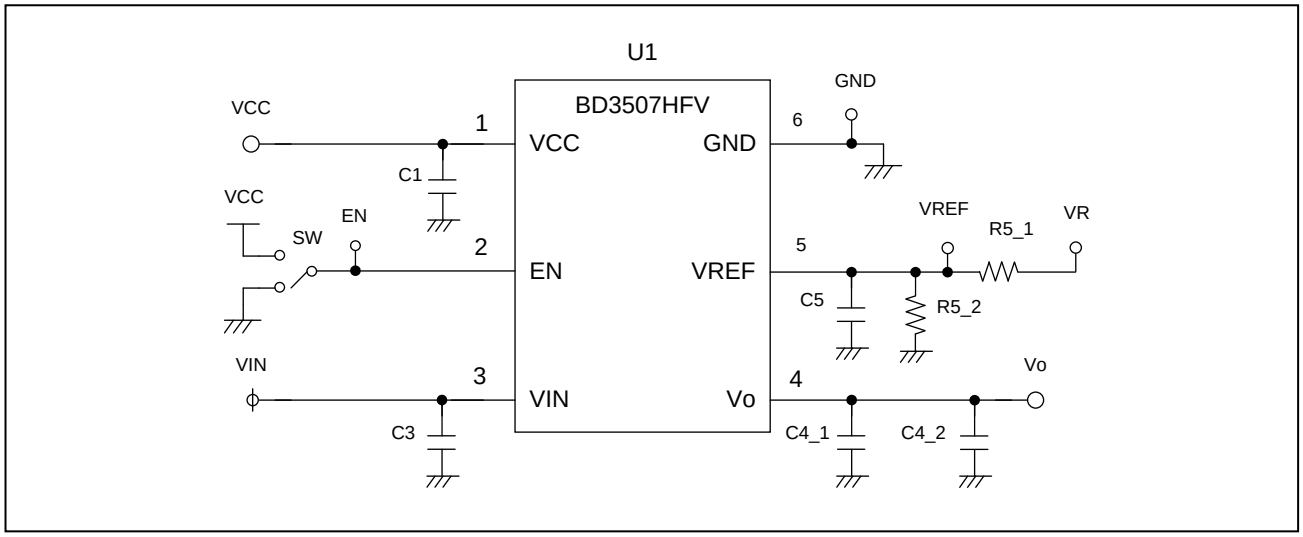
●**Application setting method**



Part No	Value	Notes for Use
R1/R2	22k/11k	The present IC can set output voltage by external reference voltage (V_R) and value of output voltage setting resistors (R1, R2). Output voltage can be set by VRxR2/(R1+R2) but it is recommended to use at the resistance value (total: about 10 kΩ) which is not susceptible to VREF bias current (±100nA).
C3	22μF	Connect the output capacitor between Vo terminal and GND terminal without fail in order to stabilize output voltage. The output capacitor has a role to compensate for the phase of loop gain and to reduce output voltage fluctuation when load is rapidly changed. When there is an insufficient capacity value, there is a possibility to cause oscillation, and when the equivalent serial resistance (ESR) of the capacitors is large, output voltage fluctuation is increased when load is rapidly changed. About 22μF ceramic capacitors are recommended but output capacitor greatly depends on temperature and load conditions. In addition, when various capacitors are connected in series, the total phase allowance of loop gain becomes not sufficient, and oscillation may result. Thoroughgoing confirmation at application temperature and under load range conditions is requested.
C1	0.1μF	The input capacitor plays a part to lower output impedance of a power supply connected to input terminals (Vcc). When output impedance of this power supply increases, the input voltages (Vcc, VIN) become unstable and there is a possibility of giving rise to oscillation and degraded ripple rejection characteristics. The use of capacitors of about 10μF with low ESR, which provide less capacity value changes caused by temperature changes, is recommended, but since input capacitor greatly depends on characteristics of the power supply used for input, substrate wiring pattern, thoroughgoing confirmation under the application temperature and load range, is requested.
C2	10μF	The input capacitor plays a part to lower output impedance of a power supply connected to input terminals (V_{IN}). When output impedance of this power supply increases, the input voltages (Vcc, V_{IN}) become unstable and there is a possibility of giving rise to oscillation and degraded ripple rejection characteristics. The use of capacitors of about 10μF with low ESR, which provide less capacity value changes caused by temperature changes, is recommended, but since input capacitor greatly depends on characteristics of the power supply used for input, substrate wiring pattern, thoroughgoing confirmation under the application temperature and load range, is requested.
C4	1μF	The present IC can set the output voltage buildup time by V_{REF} terminal capacitor (C4) and R1 and R2 values. When EN terminal is “High” or UVLO is reset, output voltage is built up by the time constant determined by C4, R1, and R2. It is recommended to use capacitors (B special) with little capacity value change caused by temperature change for C4.

●Directions for pattern layout of PCB

■ BD3507HFV Evaluation Board Circuit



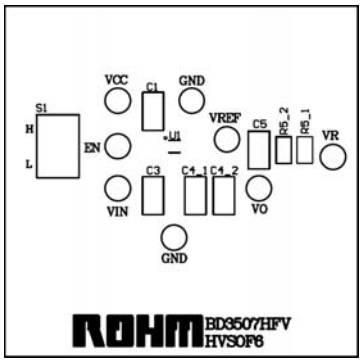
■ BD3507HFV Evaluation Board Application Components

Part No	Value	Company	Parts Name
U1	-	ROHM	BD3507HFV
R5_1	22k	ROHM	MCR03 Series
R5_2	11k	ROHM	MCR03 Series

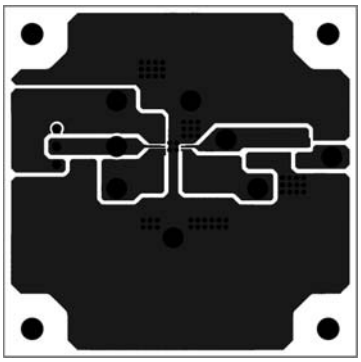
Part No	Value	Company	Parts Name
C1	1μF	MURATA	GRM18 Series
C3	10μF	MURATA	GRM21 Series
C4_1	22μF	MURATA	GRM31 Series
C4_2			
C5	1μF	MURATA	GRM18 Series

■ BD3507HFV Evaluation Board Layout

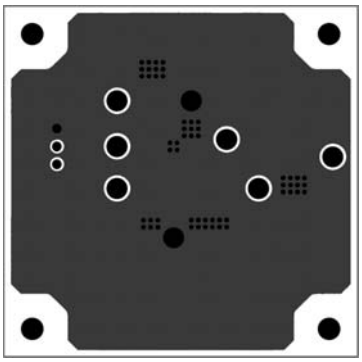
Silk Screen



TOP Layer



Mid Layer 1



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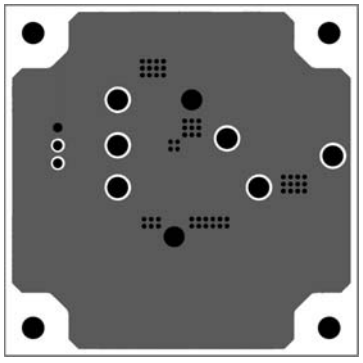

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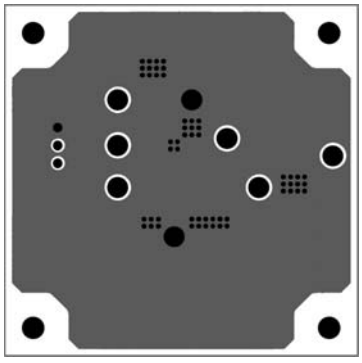


●About heat loss

In designing heat, operate the apparatus within the following conditions.
(Because the following temperatures are warranted temperature, be sure to take margin, etc. into account.)

1. Ambient temperature Ta shall be not more than 100°C.
2. Chip junction temperature Tj shall be not more than 150°C.

Chip junction temperature Tj can be considered under the following two cases.

①Chip junction temperature Tj is found from IC surface temperature TC under actual application conditions:

$Tj=TC+\theta j\text{-}c\times W$

＜Reference value＞

θj-c:HVSOF6 30℃/W

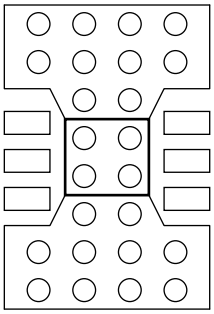
②Chip junction temperature Tj is found from ambient temperature Ta:

$Tj=Ta+\theta j\text{-}a\times W$

＜Reference value＞

θj-a:HVSOF6	243.9℃/W	Single-layer substrate (substrate surface copper foil area: less 3%)
	147.1℃/W	Single-layer substrate (substrate surface copper foil area:100mm^2)
	89.3℃/W	Single-layer substrate (substrate surface copper foil area:900mm^2)
	73.5℃/W	Single-layer substrate (substrate surface copper foil area:2500mm^2) Substrate size 70×70×1.6mm^3

When multilayer substrates are used, if any GND pattern is present in the inner layer, arrange heat radiation vias on the package rear side. Because the present package size is as small as 1.0 x 1.6 mm and vias are unable to be arranged in a large quantity at the lower part of IC, the pattern is expanded as illustrated below and the number of vias is increased to obtain superb heat radiation characteristics (the figure below is an image figure only, and the size and the quantity of vias that match the condition must be designed into patterns).



Most of heat loss in BD3507HFV occurs at the output N-channel FET. The power lost is determined by multiplying the voltage between VIN and Vo by the output current. Confirm the VIN and Vo voltages used and output current conditions, and check with the thermal derating characteristics. As this IC employs the power PKG, the thermal derating characteristics significantly depends on the pc board conditions. When designing, care must be taken to the size of a pc board to be used.

Power dissipation (W) = {Input voltage (VIN) – Output voltage (V0≒VREF)}×Io (averaged)

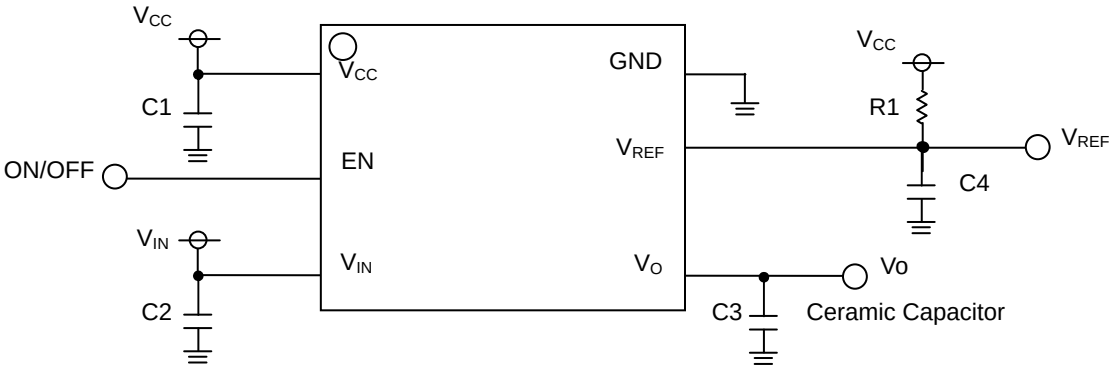
Ex.) If VIN = 1.8 volts, V0=1.2 volts, and Io (averaged)=0.5 A, the power dissipation is given by the following:

Power dissipation (W) =(1.8 volts – 1.2 volts) × 0.5 (A)
= 0.3 W

●Example of applied circuit

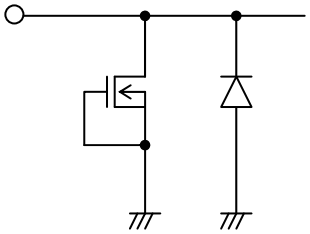
Specifications: High side switch of low-voltage power supply line (1.2-2.5V)
Characteristics: RON = 300 mΩ, Io max) = 550 mA, with soft start function and overheat protection circuit equipped.

Example Circuit

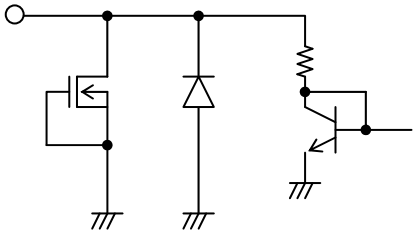


●Equivalent Circuit

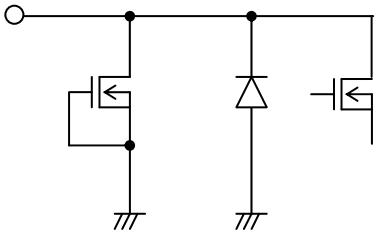
1pin (V_{CC})



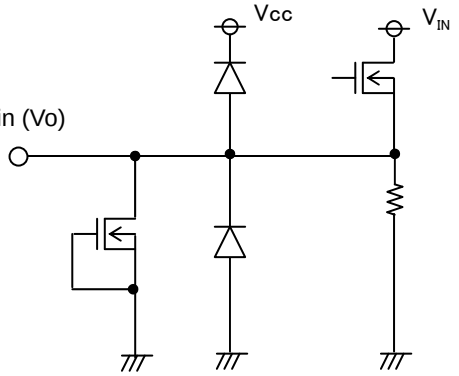
2pin (EN)



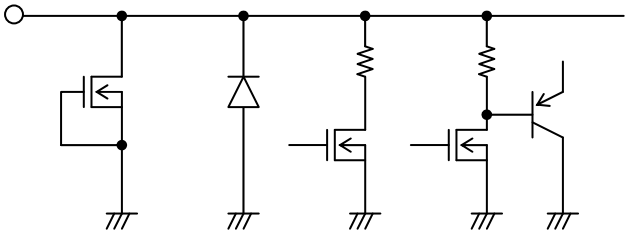
3pin (V_{IN})



4pin (Vo)



5pin (V_{REF})



●Notes for use

1. Absolute maximum ratings
   For the present product, thoroughgoing quality control is carried out, but in the event that applied voltage, working temperature range, and other absolute maximum rating are exceeded, the present product may be destroyed. Because it is unable to identify the short mode, open mode, etc., if any special mode is assumed, which exceeds the absolute maximum rating, physical safety measures are requested to be taken, such as fuses, etc.

2. GND potential
   Bring the GND terminal potential to the minimum potential in any operating condition.

3. Thermal design
   Consider permissible dissipation (Pd) under actual working condition and carry out thermal design with sufficient margin provided.

4. Terminal-to-terminal short-circuit and erroneous mounting
   When the present IC is mounted to a printed circuit board, take utmost care to direction of IC and displacement. In the event that the IC is mounted erroneously, IC may be destroyed. In the event of short-circuit caused by foreign matter that enters in a clearance between outputs or output and power-GND, the IC may be destroyed.

5. Operation in strong electromagnetic field
   The use of the present IC in the strong electromagnetic field may result in maloperation, to which care must be taken.

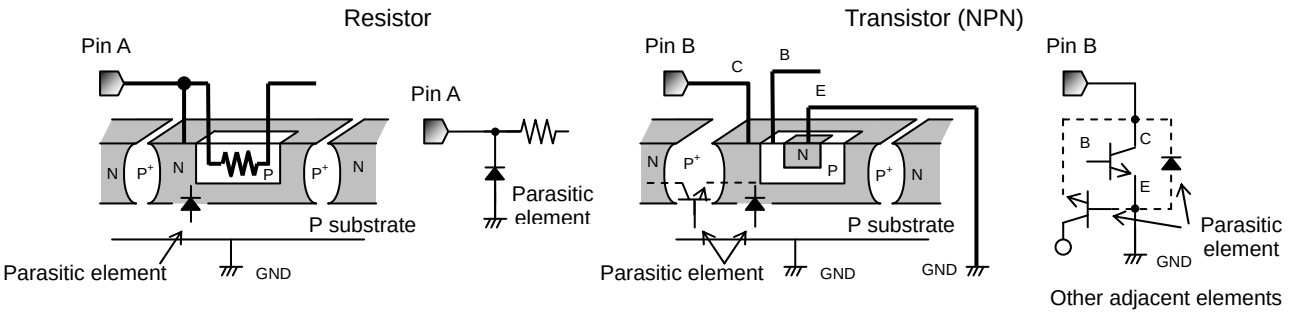
6. Built-in thermal shutdown protection circuit
   The present IC incorporates a thermal shutdown protection circuit (TSD circuit). The working temperature is 175°C (standard value) and has a -15°C (standard value) hysteresis width. When the IC chip temperature rises and the TSD circuit operates, the output terminal is brought to the OFF state. The built-in thermal shutdown protection circuit (TSD circuit) is first and foremost intended for interrupt IC from thermal runaway, and is not intended to protect and warrant the IC. Consequently, never attempt to continuously use the IC after this circuit is activated or to use the circuit with the activation of the circuit premised.

7. Capacitor across output and GND
   In the event a large capacitor is connected across output and GND, when Vcc and VIN are short-circuited with 0V or GND for some kind of reasons, current charged in the capacitor flows into the output and may destroy the IC. Use a capacitor smaller than 1000µF between output and GND.

8. Inspection by set substrate
   In the event a capacitor is connected to a pin with low impedance at the time of inspection with a set substrate, there is a fear of applying stress to the IC. Therefore, be sure to discharge electricity for every process. As electrostatic measures, provide grounding in the assembly process, and take utmost care in transportation and storage. Furthermore, when the set substrate is connected to a jig in the inspection process, be sure to turn OFF power supply to connect the jig and be sure to turn OFF power supply to remove the jig.

9. IC terminal input
   The present IC is a monolithic IC and has a P substrate and P^+ isolation between elements.
   With this P layer and N layer of each element, PN junction is formed, and when the potential relation is
   - GND>terminal A>terminal B, PN junction works as a diode, and
   - Terminal B>GND terminal A, PN junction operates as a parasitic transistor.

   The parasitic element is inevitably formed because of the IC construction. The operation of the parasitic element gives rise to mutual interference between circuits and results in malfunction, and eventually, breakdown. Consequently, take utmost care not to use the IC to operate the parasitic element such as applying voltage lower than GND (P substrate) to the input terminal.



10. GND wiring pattern
If there are a small signal GND and a high current GND, it is recommended to separate the patterns for the high current GND and the small signal GND and provide a proper grounding to the reference point of the set not to affect the voltage at the small signal GND with the change in voltage due to resistance component of pattern wiring and high current. Also for GND wiring pattern of component externally connected, pay special attention not to cause undesirable change to it.

11 Input terminals (V_{CC},V_{IN},EN,V_{REF})
In the present IC, EN terminal, V_{IN} terminal, VCC terminal, and V_{REF} terminal have an independent construction. In addition, in order to prevent malfunction at the time of low input, the UVLO function is equipped with the VCC terminal. They begin to start output voltage when all the terminals reach threshold voltage without depending on the input order of input terminals.

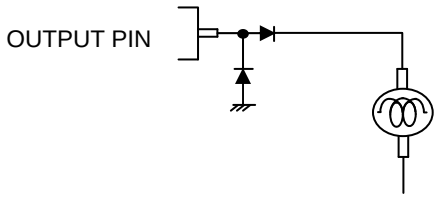
12. Heat sink
Heatsink is connected to SUB, which should be short-circuited to GND. Solder the heatsink to a pc board properly, which offers lower thermal resistance.

13. Operating range
Within the operating range, the operation and function of the circuits are generally guaranteed at an ambient temperature within the range specified. The values specified for electrical characteristics may not be guaranteed, but drastic change may not occur to such characteristics within the operating range.

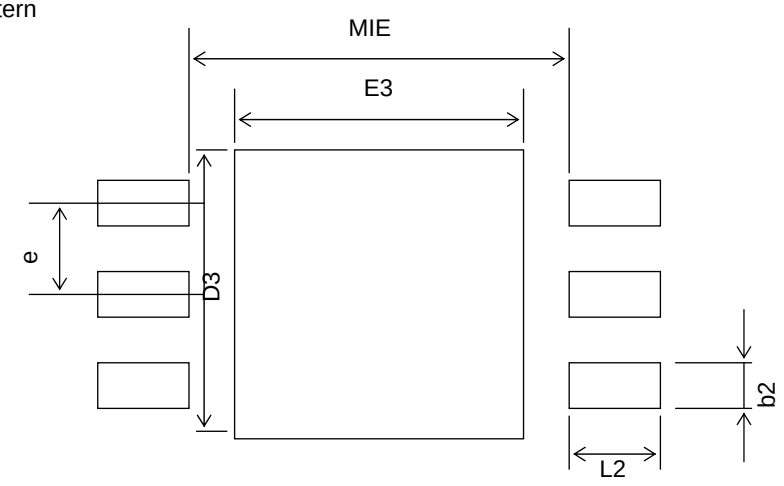
14. For the present product, thoroughgoing quality control is carried out, but in the event that applied voltage, working temperature range, and other absolute maximum rating are exceeded, the present product may be destroyed. Because it is unable to identify the short mode, open mode, etc., if any special mode is assumed, which exceeds the absolute maximum rating, physical safety measures are requested to be taken, such as fuses, etc.

15. In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.

(Example)



HVSOF6 land pattern



Unit:mm

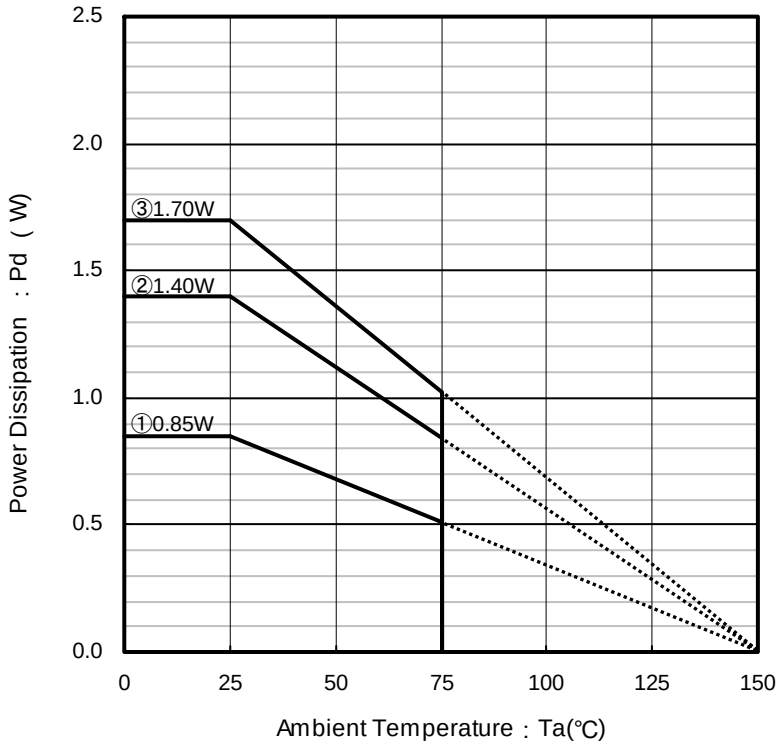
Land Pitch e	Land Space MIE	Land Length l2	Land Width b2
0.50	2.20	0.55	0.25

Pad Length D3	Pad Width E3
1.60	1.60

In actually designing, optimize in accordance with the condition.

●Power Dissipation

HVSOF 6



①:PCB 1_{st} layer (Cu-area : 100mm^2)
θ ja = 147.1℃/W
②:PCB 1_{st} layer (Cu-area : 900mm^2)
θ ja = 89.3℃/W
③:PCB 1_{st} layer (Cu-area : 2500mm^2)
θ ja = 73.5℃/W

PCB size : 70mm × 70mm × 1.6mm

●Ordering part number

B	D	3	5	0	7	H	F	V	-	T	R

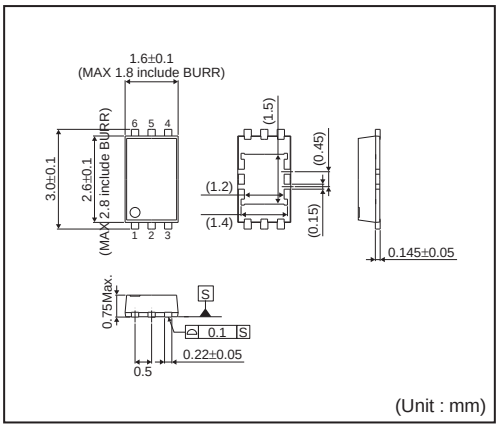
Part No. (BD)

Part No. (3507)

Package
HFV : HVSOF6

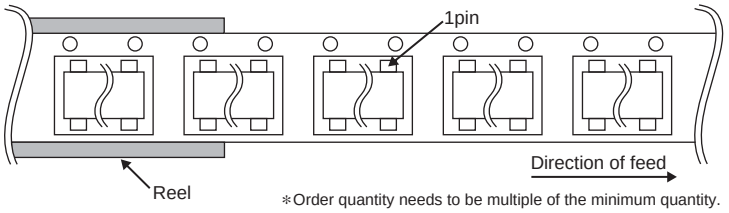
Packaging and forming specification
TR: Embossed tape and reel

HVSOF6



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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